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(54) Single gate oxide high to low level converter circuit with overvoltage protection

(57) An input stage circuit and method provides voltage level conversion and overvoltage protection for an input stage circuit using a single gate oxide pass circuit and a single gate oxide voltage level shifting circuit. In one embodiment, the circuit and method includes receiving an input signal through the single gate oxide voltage pass circuit wherein the input signal can have a voltage level higher and lower than a first reference voltage for the voltage pass circuit. An output signal from the voltage pass circuit is provided to a single gate oxide voltage level shifting circuit that shifts a voltage level of the input signal from a first logic high level to a second lower logic high level when the input signal is above a reference voltage. The circuit and method provides a scaled output signal that has a maximum voltage level substantially equal to a reference voltage associated with the level shifting circuit when the input signal exceeds the reference voltage so that an output signal to a protected circuit, such as a core logic circuitry, is above an input signal less a threshold voltage drop that occurs through the voltage pass circuit. In another embodiment, hysteresis is added for an output signal from the voltage level shifting circuit to provide suitable noise reduction prior to the converted signal being passed to subsequent stages.

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Description

[0001] The invention relates generally to over voltage protection circuits for protecting other circuits from higher than desired voltage levels, and more particularly to voltage scaling circuits for protecting an input to a protected circuit.

[0002] With the continued demand for higher speed and lower power consumption integrated circuits a need exists for simple, low cost and reliable over voltage protection circuits. For example, CMOS based video graphics chips with 128 input/output ports (I/O) ports or more are required to operate at clock speeds of 125 MHz to 250 MHz or higher. Such devices may use a 2.5 V power supply for much of its logic to reduce power consumption. One way to increase the operating speed of such devices is to decrease the gate length of core circuitry transistors. However, a decrease in the gate length of MOS devices can reduce the gate breakdown voltage to lower levels. For example, where an integrated circuit contains digital circuitry that operates from a 2.5 V source and is fabricated using silicon dioxide gate thickness of 50 Angstroms, a resulting gate breakdown voltage may be approximately 3.5 volts. Such IC's must often connect with more conventional digital devices that operate at 5 V or 3.3 V. A problem arises when the core logic circuitry (operating at 2.5 volts) receives 5 V digital input signals from peripheral devices on input pins. Such standard 5 V input signals or 3.3 V input signals can cause breakdown damage if suitable voltage protection is not incorporated.

[0003] FIG. 1 shows a known over voltage protection arrangement that attempts to overcome this problem. As seen, a resistor R is placed in the input path from an input pin P to the input I of a MOS based core logic stage, such as an input/output port on a CPU or other processing unit. A clamping diode D is placed across the input I of the core logic stage and is connected to a 2.5 V supply voltage used by the core logic to clamp over voltages coming from pin P. In operation, resistor R restricts current flow to the core logic circuit and a voltage drop occurs across the resistor. When an input voltage is high enough to cause the diode D to conduct, the diode clamps the input voltage to a fixed level (2.5 V + diode junction voltage drop). Several problems arise with such a configuration. If the core logic is fabricated with gate oxide thickness of 50 angstroms, a breakdown voltage of only 3.5 volts is required to damage the core logic stage (0.7V/A*50a = 3.5 V). With the diode drop of approximately .7 volts, a 3.2 V input voltage is a maximum input voltage to the core logic stage, however this is very close to the 3.5 V breakdown voltage so that over temperature and time, circuit reliability may be compromised. Also, the clamp diode D allows additional current to flow through the substrate which can cause latch-up of core logic circuitry.

[0004] Another problem is the use of resistor R. Such resistive elements take up large areas on integrated circuits and dissipate large amounts of power, hence heat, when an input voltage such as 5 volts is placed on pin P. In addition, a large time delay can occur due to the resistor R and the parasitic capacitance of the gate junction of the core logic circuit. This time delay reduces the speed of operation of the system.

[0005] Other overvoltage protection circuits are known, such as those disclosed in U.S. Patent No. 5,905,621 entitled "Voltage Scaling Circuit for Protecting an Input Node to a Protected Circuit," which may include single gate oxide overvoltage protection circuits. Such circuits may be quite useful in many applications. However, in the embodiment where an input voltage is provided to an nmos voltage pass device, the output from the overvoltage protection circuit may be limited to a gate supply voltage minus a threshold voltage of the voltage pass device. However, with protected circuits having lower source voltages, for example, it may be desirable to have the output of the protection circuit without any additional threshold voltage drop.

[0006] Another known overvoltage protection circuit is disclosed, for example, in U.S. Patent No. 5,319,259, entitled "Low Voltage Input and Output Circuits With Overvoltage Protection," issued on June 7, 1994. Such a circuit utilizes among other things, a feedback path to attempt to pull up an output of a protection circuit which serves as the input to another stage. However, such a circuit can start to consume current when the voltage input switches from a high level to a low level. As such, the protection circuit may unnecessarily consume current if, for example, the input stage providing the input signal does not have sufficient drive current to adequately switch an input pass transistor.

[0007] Consequently there exists a need for a single gate oxide protection circuit that reduces power consumption, improves the speed of operation of a system in a simple and reliable manner. It would desirable if the protection circuit provided, when needed, an output voltage that was substantially the same as the reference voltage of protection circuit without input current consumption as well as without DC current consumption.

[0008] According to a first aspect of the present invention, an input stage circuit that provides voltage level conversion and includes overvoltage protection comprising:

a voltage pass circuit having a first terminal operatively coupled to receive a first reference voltage, a second terminal operatively coupled to receive an input signal that can have a voltage level higher and lower than the reference voltage, and a third terminal, wherein the voltage pass circuit is made of a single gate oxide thickness; and

a single gate oxide voltage level shifting circuit having a single gate oxide overvoltage protection circuit operatively coupled between the third terminal of the voltage pass circuit and an output signal terminal of the voltage level shifting circuit, and wherein

the voltage level shifting circuit is operative to provide a scaled output signal that has a maximum voltage level substantially equal to the second reference voltage when the input voltage exceeds the second reference voltage.

[0009] According to a second aspect of the present invention, an input stage circuit comprises the steps of:

receiving an input signal through a single gate oxide voltage pass circuit wherein the input signal can have a voltage level higher and lower than a first reference voltage for the voltage pass circuit; and

shifting a voltage level of the input signal from first logic high level to a second lower logic high level through a single gate oxide voltage level shifting circuit operatively coupled to a second reference voltage and also having a single gate oxide overvoltage protection circuit, to provide a scaled output signal that has a maximum voltage level substantially equal to the second reference voltage when the input signal exceeds the second reference voltage.

[0010] The invention will be more readily understood by way of example with reference to the drawings wherein:

FIG. 1 is a prior art overvoltage protection circuit;

FIG. 2 is a block diagram illustrating one example of the invention in accordance with one embodiment of the invention;

FIG. 3 is one example of the voltage scaling circuit in accordance with one embodiment of the invention; and

FIG. 4 is a circuit diagram illustrating the circuit of FIG. 3 also employing a Schmidt trigger circuit to reduce noise.

[0011] Briefly, an input stage circuit and method provides voltage level conversion and overvoltage protection for an input stage circuit using a single gate oxide pass circuit and a single gate oxide voltage level shifting circuit. In one embodiment, the circuit and method includes receiving an input signal through the single gate oxide voltage pass circuit wherein the input signal can have a voltage level higher and lower than a first reference voltage for the voltage pass circuit. An output signal from the voltage pass circuit is provided to a single gate oxide voltage level shifting circuit that shifts with the help of inverter a voltage level of the input signal from a first logic high level to a second lower logic high level when the input signal is above a reference voltage. The circuit and method provides a scaled output signal that has a maximum voltage level substantially equal to a reference voltage associated with the level shifting circuit when the input signal exceeds the reference voltage so that an output signal to a protected circuit, such as a core logic circuitry, is above an input signal less a threshold voltage drop that occurs through the voltage pass circuit. In another embodiment, hysteresis is added for an output signal from the voltage level shifting circuit to provide suitable noise reduction prior to the converted signal being passed to subsequent stages.

[0012] FIG. 2 illustrates one example of an input stage circuit 200 that may be employed in any suitable circuit. For example, the input stage circuit 200 may be used as an interface to core circuitry that has a power supply of 2.5 V or any other suitable voltage level in an integrated circuit, such as a video and/or graphics processing circuit, microprocessor or any other suitable integrated circuit. The input stage circuit 200 is designed to receive a plurality of different voltage ranges such as 0 to 5 V, 0 to 3.3 V, 0 to 2.5 V, or any other suitable voltage range. Accordingly, the input stage circuit 200 allows interfacing to different circuits that may supply such voltage levels. This can allow the input stage circuit 200 to interface to newer and older circuits and circuits having different power supply levels and output signal levels.

[0013] The input stage circuit 200 includes a voltage pass circuit 202 with overvoltage protection, and a single gate oxide voltage level shifting circuit 204 with overvoltage protection. An inverter 206 or any other suitable logic at the output of the shifting circuit 204 provides non inverted output 220 to the core logic or other logic circuits. The voltage pass circuit 202 is made up of one or more single gate oxide devices having the same gate oxide thickness as the devices making up the single gate oxide voltage level shifting circuit 204. Accordingly, the input stage circuit 200 offers an advantage, among others, in maintaining a single fabrication process for all components therein. Preferably, the single gate oxide devices are the same gate oxide thickness as the circuit to which it provides a scaled output voltage 220. The external circuitry receiving the scale output voltage 220 includes, for example, core logic circuitry or any other suitable logic. The voltage pass circuit 202 is made of a single gate oxide thickness and includes a first terminal operatively coupled to receive a first reference voltage 210. As used herein, the term "terminal" can be any wire, pad, junction, trace, or any other suitable mechanism that allows coupling, either directly or indirectly, to receive electrical or optical energy. In addition, the voltage pass circuit 202 includes a second terminal operatively coupled to receive an input signal 212 that can have a voltage level higher and lower than the reference voltage 210. The voltage pass circuit 202 outputs a passed voltage 214 out a third terminal.

[0014] The reference voltage 210 is set at a level to provide a gate to source or gate to drain voltage within

acceptable normal operating ranges. This provides overvoltage protection for the voltage pass circuit 202.

[0015] The single gate oxide voltage level shifting circuit 204 is operative to provide a scaled output signal 208 that has a maximum voltage level substantially equal to a reference voltage 216. The single gate oxide voltage level shifting circuit 204 includes a terminal for receiving a passed voltage 214 and an output signal terminal that outputs the scale output voltage 208.

[0016] FIG. 3 illustrates an example of one embodiment of the input stage circuit 200. In this embodiment, the voltage pass circuit 202 includes an nmos transistor device 301 having a gate as a first terminal, a source as a second terminal to provide the passed voltage 214, and a drain as a third terminal to receive the variable input signal 212.

[0017] The single gate oxide voltage level shifting circuit 204 includes a terminal 300 operatively coupled to the reference voltage 216, a terminal 302 operatively coupled to receive the input signal 212, and a terminal 304 operatively coupled to the third terminal of the voltage pass circuit to receive the passed voltage 214. The single gate oxide voltage level shifting circuit 204 in this embodiment includes a pmos transistor 310, a voltage protection pmos transistor 312 and an nmos transistor 314. The pmos transistor 310 has a gate operatively coupled to receive the input signal 212, a source operatively coupled to the reference voltage 216 and a drain operatively coupled to a source of the pmos transistor 312. The pmos transistor 312 has a gate operatively coupled to the source of the nmos pass transistor and a drain operative to provide a scaled output signal. The drain is also coupled to the source of nmos transistor 314. The nmos transistor 314 has a source that also provides scaled output signal 208, a gate operatively coupled to receive the passed input voltage, and operatively coupled to the source of the nmos transistor pass circuit, and a drain operatively coupled to ground. The transistors 310, 312, 314 and the pass transistor 301 are fabricated as single gate oxide devices, preferably having a gate oxide thickness of less than 50 Å. It will be recognized that any suitable transistor configuration may also be used, if desired. In addition, coupling may be either direct or indirect depending upon the desired implementation of the circuit.

[0018] The reference voltage 216 may be, for example, a 2.5 V core logic supply voltage or any other suitable reference voltage. The reference voltage 210 may be, for example, the same voltage as the reference voltage 216 but isolated from the reference voltage 216, if desired.

[0019] In operation, the input stage circuit 200 and inverter 206 outputs the scaled output voltage 220 to be substantially equal in voltage range to the input voltage range 212 when, for example, the input voltage is at a low voltage level. For example, when a variable input voltage 212 ranges from 0 to 2.5 V, the output voltage signal 208 will range from 2.5 V to 0 V. When passed to the inverter 206, the output voltage 220 to core circuitry or other circuitry, for example, will be 0 V to 2.5 V. The voltage level shifting circuit 204 together with inverter 206 provides an output voltage 220 that is substantially the same range as the input voltage at low voltage levels. Also, the maximum output voltage 208 as well as maximum output voltage 220 is substantially the same voltage as the reference voltage 216, thereby avoiding a voltage threshold drop incorporated by the voltage pass transistor 301. During overvoltage conditions, such as where the input voltage 212 goes from 0 to 5 V, transistors 310, 312 and 314 allow the full 0 V to 2.5 V range without current draw. In addition, the transistors 310, 312 and 314 are protected from overvoltage conditions by providing a gate to drain and gate to source potential within normal operating ranges for the devices.

[0020] As the input signal 212 goes from the logic 0 to a logic 1, the pass transistor 301 limits the pass voltage 214 to approximately the reference voltage 210 minus threshold voltage for all logic highs, so that transistors 301 and 314 are not damaged due to overvoltage conditions. Transistor 314 turns on, transistor 310 turns off and the output voltage 208 is forced to ground. Where, for example, the input voltage is 5 V, the voltage at node N1 is kept low enough to avoid damage to transistors 310 and 312 during such overvoltage conditions (e.g., where the reference voltage is, for example, 2.5 V and the input logic high voltage is 5 V). However, the voltage at N1 needs to be high enough to keep the transistor 312 off but not too low to damage the gate to drain path. When transistor 310 is off, there is no current through transistor 312. In that case transistor 312 gate to source voltage is lower than, for example, the passed voltage 214 plus transistor 312 threshold voltage (in this example, this sum is ~ 2.5V). Transistor 312 isolates transistor 314 and transistor 310 drains. When transistor 314 is in an "on" condition and transistor 310 is in an "off" condition, transistor 310 gate to drain voltage would be 5V without transistor 312 isolation. In that case single gate oxide transistor 310 would be damaged.

[0021] As such, the circuit operates so that when the input voltage is 0 V, the passed voltage 214 is approximately 0 V, the output voltage is approximately 2.5 V (208) the voltage at N1 is approximately 2.5 V. The output to the core is 0 V after being inverted. In addition, the transistor 310 is "on", transistor 314 is "off', transistor 310 is "on", and transistor 312 is "on". When the input voltage is 5 V, the passed voltage is approximately 1.8 V, the output voltage 208 is approximately 0 V since transistor 314 is on. The voltage at N1 is 2.5 V, which is high enough to avoid damage between the gate and drain transistor 310 as well as the source to gate transistor 312. This is also low enough to keep the transistor 312 off. The output voltage to the core is 2.5 V after being inverted.

[0022] FIG. 4 shows another embodiment of the circuit 200 that includes a hysteresis circuit operatively

coupled to receive the output signal 208 to facilitate noise reduction for a scaled output signal. In this embodiment, the hysteresis circuit is in the form of a Schmidt trigger circuit having a plurality of transistors 400 and 402. As such, the output signal 208 may be suitably filtered to avoid glitches being passed through to core logic circuitry or other circuitry connected to an output of the input stage circuit 200. However, any suitable noise reduction circuitry may be used.

Claims

1. An input stage circuit that provides voltage level conversion and includes overvoltage protection comprising:

   a voltage pass circuit having a first terminal operatively coupled to receive a first reference voltage, a second terminal operatively coupled to receive an input signal that can have a voltage level higher and lower than the reference voltage, and a third terminal, wherein the voltage pass circuit is made of a single gate oxide thickness; and

   a single gate oxide voltage level shifting circuit having a single gate oxide overvoltage protection circuit operatively coupled between the third terminal of the voltage pass circuit and an output signal terminal of the voltage level shifting circuit, and wherein the voltage level shifting circuit is operative to provide a scaled output signal that has a maximum voltage level substantially equal to the second reference voltage when the input voltage exceeds the second reference voltage.

2. The circuit of Claim 1, wherein the voltage pass circuit is a transistor.

3. The circuit of Claim 1 or Claim 2, wherein the single gate oxide voltage level shifting circuit includes a fourth terminal operatively coupled to a second reference voltage, a fifth terminal operatively coupled to receive the input signal, and a sixth terminal operatively coupled to the third terminal of the voltage pass circuit.

4. The circuit of any one of the preceding claims, wherein the single gate oxide voltage pass circuit includes an nmos transistor device having a gate as the first terminal, a source as the second terminal and a drain as the third terminal.

5. The circuit of any one of the preceding claims, wherein the single gate oxide voltage level shifting circuit includes at least a first transistor operatively coupled to the second reference voltage and to the input signal, a second transistor operatively coupled to the first transistor and to the third terminal, and a third transistor operatively coupled to the second transistor and to the third terminal of the voltage pass circuit.

6. An input stage circuit that provides voltage level conversion and includes overvoltage protection comprising:

   at least an nmos voltage pass transistor having a gate operatively coupled to receive a first reference voltage, a drain operatively coupled to receive an input signal that can have a voltage level higher and lower than the first reference voltage, and a source for outputting a passed input signal; and

   a single gate oxide voltage level shifting circuit having a first pmos transistor, a second pmos transistor and an nmos transistor wherein the first pmos transistor has a gate operatively coupled to receive the input signal, a source operatively coupled to a second reference voltage, and a drain operatively coupled to a source of the second pmos transistor, and wherein the second pmos transistor has a gate operatively coupled to the source of the nmos pass transistor and a drain operative to provide a scaled output signal, and wherein the nmos transistor has a source operatively coupled to the drain of the pmos overvoltage transistor, and a gate operatively coupled to receive the passed input voltage; and
   wherein the nmos voltage pass transistor, the first pmos transistor, the second pmos transistor and the nmos transistor are fabricated as single gate oxide devices.

7. The circuit of Claim 5 or Claim 6, including a hysteresis circuit operatively coupled to the third terminal and operatively coupled to output signal terminal to facilitate noise reduction for a scaled output signal.

8. The circuit of Claim 7, wherein the hysteresis circuit is a Schmidt trigger circuit.

9. The circuit of any one of Claims 4 to 6 or any claim dependent thereon, when dependent on either Claim 2 or Claim 3 when dependent on Claim 2, wherein the transistors of the single gate oxide voltage level shifting circuit and the single gate oxide voltage pass circuit have a gate oxide thickness of 50 Å or less and wherein the input signal is one of a plurality of at least three different voltage ranges.

10. A method for providing voltage level conversion and overvoltage protection for an input stage circuit

comprising the steps of:

receiving an input signal through a single gate oxide voltage pass circuit wherein the input signal can have a voltage level higher and lower than a first reference voltage for the voltage pass circuit; and

shifting a voltage level of the input signal from first logic high level to a second lower logic high level through a single gate oxide voltage level shifting circuit operatively coupled to a second reference voltage and also having a single gate oxide overvoltage protection circuit, to provide a scaled output signal that has a maximum voltage level substantially equal to the second reference voltage when the input signal exceeds the second reference voltage.

11. The method of Claim 10 including providing hysteresis for an output signal terminal to facilitate noise reduction for a scaled output signal from the single gate oxide voltage level shifting circuit.

12. The circuit of any one of the preceding claims, wherein the first and second reference voltages are 2.5V and wherein the input signal can vary between at least 0-5V.

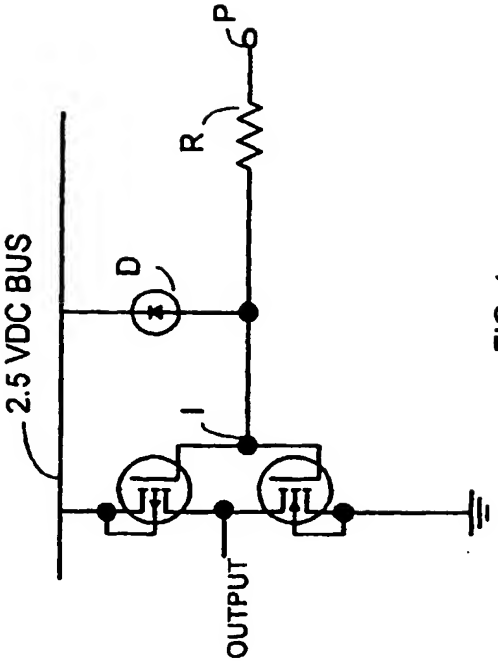

FIG. 1
PRIOR ART

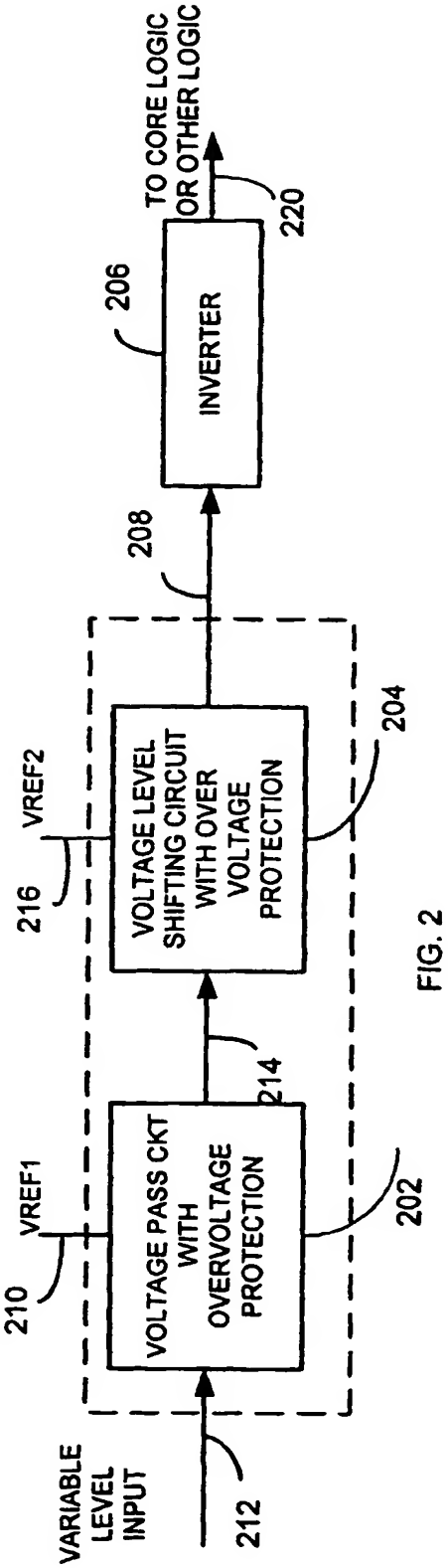

FIG. 2

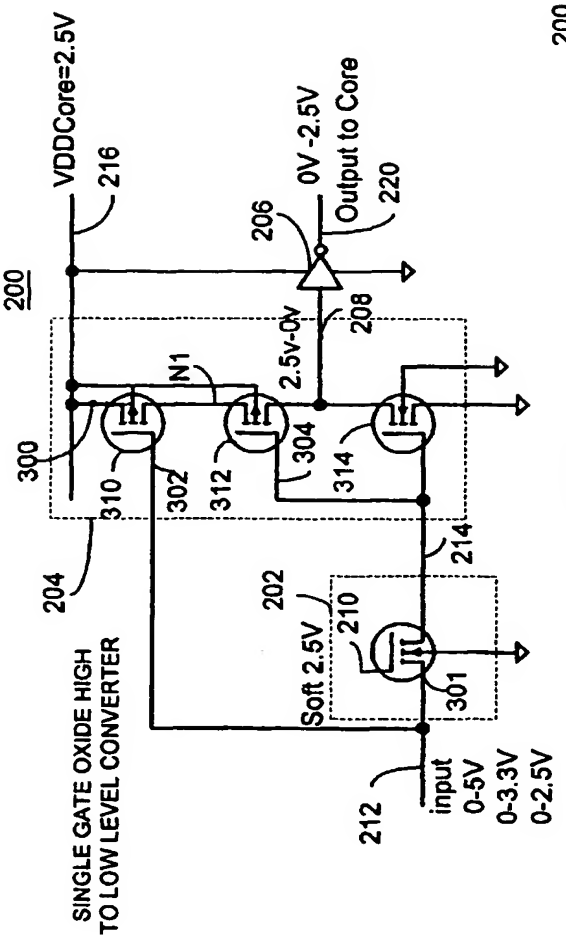

FIG. 3

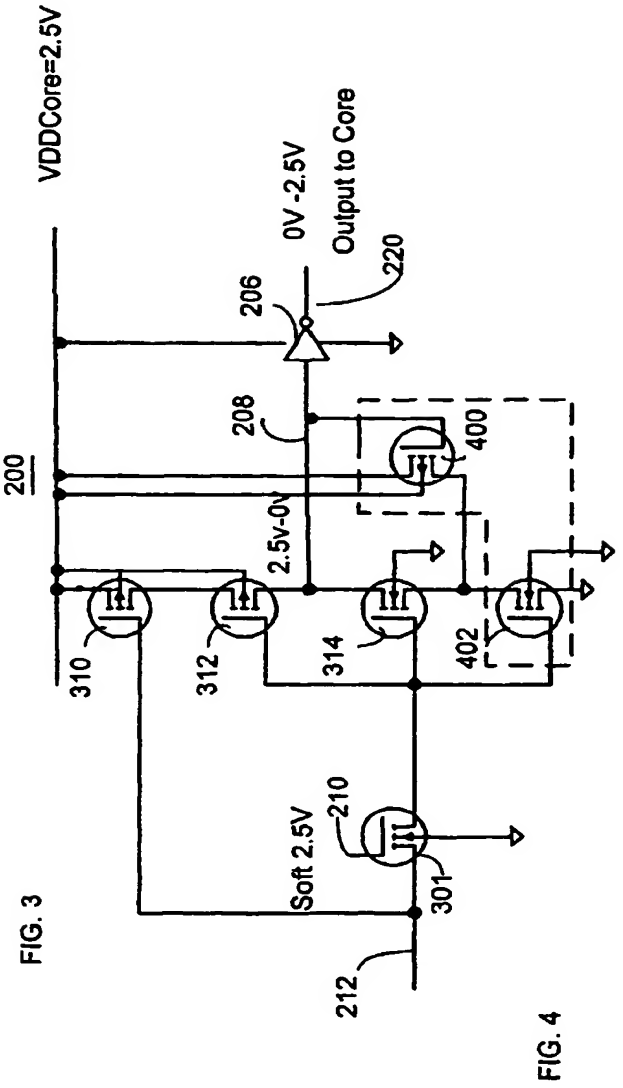

FIG. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 00 30 5690

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A,D	US 5 905 621 A (DRAPKIN OLEG) 18 May 1999 (1999-05-18) * abstract * * column 2, line 52 - line 55 * * column 2, line 62 - line 65 * * figure 3 *	1,6,10	H02M3/02 H02H3/20
A,D	US 5 319 259 A (MERRILL RICHARD B) 7 June 1994 (1994-06-07) * abstract * * column 4, line 59 - column 5, line 9 * * figure 9 *	1,6,10	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H02M
H02H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	19 October 2001	Roider, A

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19-10-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 5319259 A	07-06-1994	NONE	

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